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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	12

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/410,928	JONES ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed January 8, 2004 in response to PTO Office Action dated November 26, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-19 have been presented for examination in this application. In response to the last Office Action, claims 1-9 and 12-16 have been amended. Claims 17-19 have been added.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "cache coherency transaction defined within the transaction-based bus mechanism even when the cache memory is not coupled to the transaction-based bus mechanism" (claim 17), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8, 14, and 16-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the system devices" in line 10. There is insufficient antecedent basis for this limitation in the claim. A previous recitation of a "system devices" had not been presented. It is also unclear to the Examiner whether these "system devices" correspond, or are related to, the system components of line 9.

Claim 1 recites the limitation "main memory" in lines 10-11. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner as to the location or implementation of the "main memory" into the computer system, which is necessary in regards to the claim limitations directed towards the "direct" coupling of the main memory. Also, it is unclear to the Examiner if the "main memory" corresponds to the "shared memory" of line 3, the "memory system" of line 2, or another claim limitation.

Claim 6 recites the limitation "main memory" in lines 5 and 8-9. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner as to the location or implementation of the "main memory" into the computer system, which is necessary in regards to the claim limitations directed towards the "direct" coupling of the main memory.

Claim 8 recites the limitation "main memory" in lines 7-8 and 10-11. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner as to the location or implementation of the "main memory" into the computer system, which is necessary in regards to the claim limitations directed towards the "direct" coupling of the main memory.

Claim 14 recites the limitation "main memory" in lines 6 and 9. There is insufficient antecedent basis for this limitation in the claim. A previous recitation of a "main memory" had not been presented. It is also unclear to the Examiner as to the location or implementation of the "main memory" into the computer system, which is necessary in regards to the claim limitations directed towards the "direct" coupling of the main memory.

Claim 16 recites the limitation "main memory" in lines 8 and 12. There is insufficient antecedent basis for this limitation in the claim. A previous recitation of a "main memory" had not been presented. It is unclear to the Examiner as to the location or implementation of the "main memory" into the computer system, which is necessary in regards to the claim limitations directed towards the "direct" coupling of the main memory.

Claim 17 recites the limitation "a cache coherency transaction" in lines 2-3 and 7. It is unclear to the Examiner whether the two "a cache coherency transaction" limitations are in fact the same "a cache coherency transaction", or correspond to separate cache coherency transactions.

Claims 2-5, 7, 18, and 19 are rejected as being dependent upon a previously rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US# 6,418,514). The rejection to claim 17 is made in light of the 35 U.S.C. 112, second paragraph, rejections disclosed above.

Regarding claim 17, the cache operations queue (68a) and corresponding buses (including system bus (54)) of Arimilli et al., connecting the queue to various system components, corresponds to the **transaction-based bus *mechanism*** (emphasis

added), as claimed. The transaction-based bus mechanism is not limited to containing only signal lines, since the claim recites that cache coherency transactions must also be present and stored within the mechanism. The queue (68a) is indirectly **coupled to the memory system** via unmarked internal buses (seen in Fig. 7) and system bus (54). The operations queue contains a serialized list of cache operations that results in a bus transaction (col. 13, lines 29-35). Arimilli et al. also teaches including the **MESI cache coherency protocol** within the multi-processor computer system (abs., lines 1-2), where the Shared (S) value corresponds indicates that two or more caches each hold a valid copy of a memory block (col. 8, lines 43-55).

A **processor** is connected to the cache (col. 13, lines 26-28), or contains the cache (Figs. 1 & 6), which is **coupled to the memory system via system bus** (54). For example, **caches (24) and (26) are not directly coupled to the system bus**, here (20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US# 6,418,514) in view of Applicant's Admitted Prior Art (AAPA). The rejections to claims 1-4,18 and 19 are made in light of the 35 U.S.C. 112, second paragraph, rejections disclosed above.

Regarding claim 1, Arimilli et al. teaches a **computer system** including a **memory system** (memory device (16)). **Memory device (16)**, as well as (52), are **shared and used by multiple processing** units to carry out program instructions.

The cache operations queue (68a) and corresponding buses (including system bus (54)) connecting the queue to various system components corresponds to the **transaction-based bus *mechanism*** (emphasis added), as claimed. The transaction-based bus mechanism is not limited to containing only signal lines, since the claim recites that cache coherency transactions must also be present and stored within the mechanism. The queue (68a) is indirectly **coupled to the memory system** via unmarked internal buses (seen in Fig. 7) and system bus (54). The operations queue contains a serialized list of cache operations that results in a bus transaction (col. 13, lines 29-35). Arimilli et al. also teaches including the **MESI cache coherency protocol** within the multi-processor computer system (abs., lines 1-2), where the Shared (S) value corresponds indicates that two or more caches each hold a valid copy of a memory block (col. 8, lines 43-55).

A **processor** is connected to the cache (col. 13, lines 26-28), or contains the cache (Figs. 1 & 6), which is **coupled to the memory system via system bus** (54).

Figure 7 also illustrates other **system components** (cache logic (64a), LRU (62a)), etc.) coupled to the cache operations queue. The claim limitation "coupled" is not limited to the coupling of system components with a direct connection to the cache operations queue.

A **(first) cache coherency request**, issued by a processor or higher-level cache associated with cache (56a) is made in order to claim exclusive ownership of a memory block, where exclusive ownership corresponds to the coherency aspect of the claim limitation. The operation is posted in the operations queue, and then the processor or higher-level cache issues one or more instructions in order to carry out the cache coherency command that was placed in the operations queue (col. 13, lines 44-54). Another operation regarding multi-processor cache line requesting to another cache is also taught by Arimilli et al. (col. 12, lines 17-24). Thus, **in response to the request**, the cache coherency operation is performed.

Regarding claim 1, Arimilli et al. does not teach that system components other than the processor are coupled to the transaction-based bus mechanism, where the system devices access main memory directly through the transaction-based bus mechanism, but do not access the cache memory directly through the transaction-based bus mechanism. AAPA teaches **that non-processor devices (DMA devices) can access the main memory directly, but do not access the cache directly** (page 3, lines 24-26). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al. and AAPA before him at the time the invention was made to modify the computing system of Arimilli et al. to include the non-processor

device functionality of AAPA, because then efficient use of the processor could be obtained, as taught by AAPA (page 3, line 12-14).

Regarding claim 9, Arimilli et al. teaches a **computer system** including a **shared memory system** (memory device (16)). **Memory device (16)**, as well as (52), are **shared and used by multiple processing** units **(modules)** to carry out program instructions. As seen in Figure 7, the processors are coupled to caches (56(a)) and (56(b)), which are in turn coupled to system bus (54). The **caches are used for storing information from the memory device** that is useful to the processor (col. 1, lines 61-65).

A **(first) cache coherency request**, issued by a processor or higher-level cache associated with cache (56a) is made in order to claim exclusive ownership of a memory block, where exclusive ownership corresponds to the coherency aspect of the claim limitation. The operation is posted in the operations queue, and then the processor or higher-level cache issues one or more instructions in order to carry out the cache coherency command that was placed in the operations queue (col. 13, lines 44-54). Another operation regarding multi-processor cache line requesting to another cache is also taught by Arimilli et al. (col. 12, lines 17-24). Thus, **in response to the request**, the cache coherency operation is performed.

Regarding claim 9, Arimilli et al. does not teach that system components other than the processor are coupled to the transaction-based bus mechanism, where the system devices access main memory directly through the transaction-based bus

mechanism, but do not access the cache memory directly through the transaction-based bus mechanism. AAPA teaches **that non-processor devices (DMA devices) can access the main memory directly, but do not access the cache directly** (page 3, lines 24-26). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al. and AAPA before him at the time the invention was made to modify the computing system of Arimilli et al. to include the non-processor device functionality of AAPA, because then efficient use of the processor could be obtained, as taught by AAPA (page 3, line 12-14).

Regarding claims 2 and 10, Arimilli et al. teaches that the first request disclosed above is performed without the use of an interrupting mechanism.

Regarding claims 3 and 11, Arimilli et al. teaches that the LRU unit (62a) is issued instructions to carry out for the purpose of selecting the memory block for eviction, which is a part of the cache coherency operation discussed above and taught by Arimilli et al. (col. 13, lines 51-54). Therefore, the LRU init (62a) operates instructions, sent from the processor, **without the assistance of instructions directly executed on the processor**.

Regarding claims 4 and 12, Arimilli et al. teaches that requesting processor (44f) is issued a command, or message, to switch a cache line's MESI value from Invalid to Recent as a **response** to a cache coherency operation (col. 12, lines 19-24).

Regarding claim 18, Arimilli et al. teaches that Figure 7 also illustrates other **system components** (cache logic (64a), LRU (62a)), etc.) coupled to the cache

operations queue. The claim limitation "coupled" is not limited to the coupling of system components with a direct connection to the cache operations queue. A **(first) cache coherency request**, issued by a processor or higher-level cache associated with cache (56a) is made in order to claim exclusive ownership of a memory block, where exclusive ownership corresponds to the coherency aspect of the claim limitation. The operation is posted in the operations queue, and then the processor or higher-level cache issues one or more instructions in order to carry out the cache coherency command that was placed in the operations queue (col. 13, lines 44-54). Another operation regarding multi-processor cache line requesting to another cache is also taught by Arimilli et al. (col. 12, lines 17-24). Thus, **in response to the request**, the cache coherency operation is performed.

Regarding claim 19, Arimilli et al. also does not teach that one of components other than the processor may be a direct memory access (DMA) controller. AAPA teaches that the "other components" may include a **DMA controller** (page 3, lines 14-17), or a DMA device (page, lines 24-26) that controls accessing the main memory.

Claims 5, 6, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US# 6,418,514) and Applicant's Admitted Prior Art (AAPA) as applied to claims 1-4, 9-12, 18 and 19 above, and further in view of Spencer (US# 6,295,582). The rejection made to claim 14 is made in light of the 35 U.S.C. 112, second paragraph, rejections disclosed above.

Regarding claims 5 and 13, Arimilli et al. and AAPA, disclosed supra, do not teach cache flush operations for flushing a cache line, as well as a hit/miss cache item scheme including a writeback operation for cache line hits with modified results. Spencer teaches a cache memory manager enabled to ensure cache space for future operations. The cache memory manager is able to **flush** one or more cache lines of data from the cache according to its own operation (col. 14, lines 2-10).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al., AAPA, and Spencer before him at the time the invention was made to modify the cache coherency scheme of Arimilli et al. and AAPA to include the flushing and write-back schemes of Spencer, because then system-wide data coherency could be maintained as well as implementing a function for consistent cache availability for future cache operations, as taught by Spencer.

Regarding claims 6 and 14, Spencer teaches a cache **miss** resulting from a **lookup** in the loading of data from a main memory into the cache (response). On a cache **hit**, the data is already in the cache in an unmodified format and able to be immediately used (col. 4, lines 45-55). On a cache write-hit to a modified line, a dirty bit is set and the cache controller is responsible for writing-back the updated data to the main memory before replacing the data related to the write-hit (col. 5, lines 13-30).

Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US# 6,418,514) and Applicant's Admitted Prior Art

(AAPA) as applied to claims 1-4, 9-12, 18 and 19 above, and further in view of Jacobs (US# 6,047,358). The rejections to claims 8 and 16 are made in light of the 35 U.S.C. 112, second paragraph, rejections disclosed above.

Regarding claims 7 and 15, Arimilli et al. and AAPA, disclosed supra, do not teach a cache purge operation for purging a cache line. As part of the copy-back operation, the cache line is marked as invalid (col. 18, lines 58-61) for eviction (**purging**) of the cache line.

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Arimilli et al., AAPA, and Jacobs before him at the time the invention was made to modify the cache coherency scheme of Arimilli et al. and AAPA to include the purging and write-back schemes of Jacob, because then system-wide data coherency could be maintained as well as a replacement policy that includes the principles of locality to reduce cache misses, as taught by Spencer.

Regarding claims 8 and 16, as well as a hit/miss cache item scheme including a writeback and invalidation system for cache line hits with modified results. Jacobs teaches that upon a cache miss resulting from a cache **lookup**, the requested item is loaded into the cache (col. 10, lines 58-62). Jacobs also teaches a write access (hit) that results in the cache line incorporating a modified value setting within a copy-back (write-back) coherency policy (col. 10, lines 34-46). As part of the copy-back operation, the cache line is marked as invalid (col. 18, lines 58-61).

Response to Arguments

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments of pages 11-12 recite that "the transaction-based bus of claim 1 is not fairly shown or suggested... in Arimilli et al.". A "transaction-based bus" is not recited in claim 1, although a "transaction-based bus *mechanism*"(emphasis added) is. Where as a bus is limited to device interconnecting signal lines, a bus mechanism may include the signal lines as well as other components together as a single mechanism.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

February 18, 2004